CLAIMS

What is claimed is:

1. A multi-chip module, comprising:

a substrate having a first side and a second side and at least two elongate through-slots extending from the first side to the second side thereof, said through-slots having a length and width;

electrical conductors formed on said first side and second side of said substrate, said electrical conductors having connection terminals adjacent said at least two through-slots for bonding portions of wires to bond pads exposed through said at least two through-slots;

electrical input/output connectors for connecting said electrical conductors to an external circuit;

a first semiconductor die having an active surface with a plurality of bond pads thereon, and a reverse surface, a portion of said active surface bonded to said first side of said substrate, at least one of the plurality of conductive bond pads on the active surface of the semiconductor die exposed through a through-slot in said substrate for bonding a portion of a wire to at least one conductor on said second side of said substrate;

a second semiconductor die having an active surface with a plurality of bond pads thereon, and a reverse surface, a portion of said active surface bonded to said first side of said substrate, at least one bond pad of the plurality of bond pads thereon exposed through a through-slot in said substrate for wire-bonding to at least one conductor on said first side of said substrate; and

at least two conductive wires connecting at least two of said bond pads on said first semiconductor die and said second semiconductor die to at least two of said connection terminals, one of said at least two connection terminals located on the first side of said substrate and the other of said at least two connection terminals located on the second side of said substrate, said first semiconductor die and said

second semiconductor die positioned wherein a conductive wire connected thereto extends through a through-slot in said substrate.

2. The multi-chip module of claim 1, further comprising glob-top sealant filling said at least two through-slots in said substrate.

3. The multi-chip module of claim 1, further comprising a layer of polymeric sealant encapsulating a portion of said module.

4. The multi-chip module of claim 1, wherein said first semiconductor die and said second semiconductor die are attached to said substrate at two different planes.

5. The multi-chip module of claim 1, wherein said electrical conductors on said first side of said substrate have connection terminals adjacent one through-slot in said substrate for wire-bonding to bond pads on said first semiconductor die attached to said second side, and said electrical conductors on said second side of said substrate have connection terminals adjacent another through-slot for wire-bonding to bond pads on said second semiconductor die attached to said first side of said substrate.

6. The multi-chip module of claim 1, wherein said electrical conductors comprise metallization patterns on said first and second sides of said substrate.

7. The multi-chip module of claim 1, further comprising:
conductive vias through said substrate and connecting electrical conductors on the first side and the second side of said substrate.

8. The multi-chip module of claim 1, wherein said electrical connectors comprise a ball-grid-array of solder balls on one side of said substrate.

9. The multi-chip module of claim 1, wherein said electrical connectors comprise an edge connector.

10. The multi-chip module of claim 1, wherein said electrical connectors comprise a socket connector.

11. A multi-chip module, comprising:

a substrate having a first side, a second side, and a plurality of elongate through-slots extending from the first side to the second side thereof, said through-slots having a length and width;

electrical conductors formed on said first side and second side of said substrate and having connection terminals adjacent said through-slots for wire-bonding to bond pads exposed through said through-slots;

electrical input/output connectors for connecting said electrical conductors to an external circuit;

a plurality of semiconductor dice, each semiconductor die of said plurality of semiconductor dice having an active surface having a plurality of bond pads thereon and a reverse surface, a plurality of said active surface bonded to said first side of said substrate, the bond pads of each semiconductor die exposed through a through-slot of said plurality of through-slots to said second side of said substrate for wire-bonding to conductors on said second side, at least one semiconductor die of said plurality of semiconductor dice attached to said second side of said substrate, the bond pads of said at least one semiconductor die of said plurality of semiconductor dice exposed through a through-slot to said first side of said substrate for wire-bonding to conductors on said first side of said substrate; and

conductive wires connecting said bond pads of said plurality of said semiconductor dice to said connection terminals, each said semiconductor die of said plurality of semiconductor dice positioned having conductive wires connected thereto extend

through a through-slot in a space between adjacent spaced dice on the opposite side of said substrate thereto.

12. The multi-chip module of claim 11, further comprising glob-top sealant covering said bond pads and conductive wires within said through-slots.

13. The multi-chip module of claim 12, wherein said glob-top sealant fills said space between adjacent semiconductor die.

14. The multi-chip module of claim 11, further comprising a layer of polymeric sealant encapsulating said module.

15. The multi-chip module of claim 11, wherein said dice are attached in a bi-planar configuration on said substrate.

16. The multi-chip module of claim 11, wherein said electrical conductors on said first side of said substrate have connection terminals adjacent alternate through-slots for wire-bonding to bond pads on semiconductor die of said plurality of semiconductor dice attached to said second side of said substrate, and said electrical conductors on said second side have connection terminals adjacent other through-slots for wire-bonding to bond pads on semiconductor die of said plurality of semiconductor dice attached to said first side.

17. The multi-chip module of claim 11, wherein said electrical conductors comprise metallization patterns on said first side and second side of said substrate.

18. The multi-chip module of claim 11, further comprising conductive vias through said substrate ~~and~~ connecting electrical conductors on opposite sides of said substrate.

19. The multi-chip module of claim 11, wherein said electrical connection means comprises a ball-grid-array of solder balls on one side of said substrate, in the periphery thereof about said attached dice.

20. The multi-chip module of claim 11, wherein said electrical connectors comprise an edge connector.

21. The multi-chip module of claim 11, wherein said electrical connectors comprise a socket connector.

22. The multi-chip module of claim 11, wherein the number of said plurality of semiconductor dice mounted on said second side of said substrate differs by one from the number of said plurality of semiconductor dice mounted on said first side of said substrate.

23. The multi-chip module of claim 11, wherein the length of said through-slot exceeds the length of said bond pads on a semiconductor die of said plurality of semiconductor dice.

24. The multi-chip module of claim 11, wherein said through-slot has uniform dimensions between said first side and said second side of said substrate.

25. The multi-chip module of claim 11, wherein the width of a through-slot of said plurality of through-slots is greater at one of said first and second sides of said substrate.

26. The multi-chip module of claim 25, wherein the width of a through-slot of said plurality of through-slots is configured to provide a step intermediate said first side and said second side of said substrate.

27. The multi-chip module of claim 26, wherein said connection terminals of the electrical conductors are positioned on said step.

28. The multi-chip module of claim 25, wherein said through-slot is beveled between said first side and second side of said substrate.

29. The multi-chip module of claim 11, wherein said bond pads of a semiconductor die of said plurality of semiconductor dice are positioned along a center line of said active surface.

30. The multi-chip module of claim 11, wherein at least two semiconductor ~~die~~ of said plurality of semiconductor dice attached to said first side of said substrate lie in a first plane and at least two semiconductor ~~die~~ of said plurality of semiconductor dice attached to said second side of said substrate lie in a second plane.

31. The multi-chip module of claim 11, ~~wherein said module comprises a~~ memory device wherein a majority of said plurality of semiconductor dice have internal circuits.

32. A method for forming a high density multi-chip module, comprising the steps of:

providing a plurality of integrated circuit semiconductor dice, each semiconductor die having an active surface having a plurality of bond pads thereon;

forming a substrate with opposing first and second sides, at least three elongate through-slots extending from said first side to said second side, each said through-slot configured for opposite side access between attached semiconductor die of said plurality of semiconductor dice to the bond pads of a semiconductor die of said plurality of semiconductor dice bonded to said substrate;

forming a pattern of a plurality of electrical conductors associated with said substrate, at least one electrical conductor of said plurality of electrical conductors having a

connection terminal adjacent a through-slot of said at least three through-slots for connecting said bond pads of a semiconductor die of said plurality of semiconductor dice to an input/output connector;

forming an input/output connector on said substrate and connecting said input/output connector to said electrical conductors;

attaching the active surfaces of a plurality of said semiconductor dice to a first side of said substrate wherein the bond pads thereof are aligned with alternate through-slots for access from the second side of said substrate;

attaching the active surface of at least one semiconductor die of said plurality of semiconductor dice to said second side of said substrate, the bond pads of said at least one semiconductor die aligned with other alternate through-slots for access from the first side of said substrate; and

wire-bonding said bond pads of each attached semiconductor die of said plurality of semiconductor dice to connection terminals adjacent the corresponding through-slot.

33. The method of claim 32, wherein ~~the step of~~ forming through-slots comprises forming an elongate stepped surface in said through-slot.

34. The method of claim 33, wherein the step of forming a pattern of electrical conductors includes forming conductive connection terminals on said stepped surface.

35. The method of claim 32, further comprising the step of:

inserting a flowable hardenable glob-top material into each said through-slot to encapsulate ~~the~~ wires therein.

36. The method of claim 35, wherein a hardenable polymeric material is inserted into said through-slot.

37. The method of claim 35, wherein said glob-top material is inserted to extend outwardly between the edges of at least two semiconductor die of said plurality of semiconductor dice proximate each side of said through-slot.

38. The method of claim 32, further comprising the step of:
performing electrical testing of said plurality of semiconductor dice following wire-bonding thereof and prior to wire encapsulation.

39. The method of claim 32, comprising the further step of:
encapsulating said dice with a polymeric sealant.

40. The method of claim 32, wherein the step of forming a pattern of electrical conductors on said substrate comprises forming a conductor pattern on each of said first side and second side of said substrate.

41. The method of claim 40, further comprising the step of:
connecting said two conductor patterns with conductive vias through said substrate.

42. The method of claim 41, wherein the step of forming an input/output connector comprises forming one of a ball-grid-array and a pin-grid-array on one of said sides in a peripheral area surrounding said plurality of semiconductor dice.

43. The method of claim 42, wherein the step of forming an input/output connector comprises forming a socket connector on an edge of said substrate.

44. A method for forming a high density multi-chip module, comprising the steps of:
providing a plurality of integrated circuit dice, each die having an active surface with a row of conductive bond pads;

forming a planar substrate with opposing first and second sides, at least three elongate through-slots extending from said first side to said second side, each said through-slot configured for opposite side access between attached dies to the conductive bond pads of a die bonded to said substrate;

forming a pattern of electrical conductors associated with said substrate and having connection terminals adjacent each said through-slot for connecting said bond pads to an input/output connection means;

forming an input/output connector on said substrate and connecting said input/output connector to said electrical conductors from said bond pads;

attaching the active surfaces of a plurality of said dice to a first side of said substrate wherein the bond pads thereof are aligned with alternate through-slots for access from the second side;

attaching the active surface of at least one of said dice to said second side of said substrate wherein the bond pads thereof are aligned with other alternate through-slots for access from the first side; and

wire-bonding said bond pads of each attached die to connection terminals adjacent the corresponding through-slot.

45. The method of claim 44, wherein ~~the step of~~ forming through-slots comprises forming an elongate stepped surface in said through-slot.

46. The method of claim ~~44~~, wherein the step of forming a pattern of electrical conductors includes forming conductive connection terminals on said stepped surface.

47. The method of claim 44, further comprising the step of inserting a flowable hardenable glob-top material into each said through-slot to encapsulate ~~the~~ wires therein.

48. The method of claim 47, wherein a hardenable polymeric material is inserted into said through-slot.

49. The method of claim 47, wherein said glob-top material is inserted to extend outwardly between ~~the~~ edges of dice proximate each side of said through-slot.

50. The method of claim 44, further comprising the step of:
performing electrical testing of said dice following wire-bonding thereof and prior to wire encapsulation.

51. The method of claim 44, comprising the ~~further~~ step of:
encapsulating said dice with a polymeric sealant.

52. The method of claim 44, wherein the step of forming a pattern of electrical conductors on said substrate comprises forming a conductor pattern on each of said first and second sides.

53. The method of claim 52, further comprising the step of:
connecting said two conductor patterns with conductive vias through said substrate.

54. The method of claim 44, wherein the step of forming an input/output connector comprises forming one of a ball-grid-array and a pin-grid-array on one of said sides in a peripheral area surrounding said dice.

55. The method of claim 44, wherein the step of forming an input/output connector comprises forming a socket connector on an edge of said substrate.